

REPLACEMENT SHEET

Fig. 1A

a0~a13

BA

Vcc

Vss

BA : BLOCK ADDRESS

Fig. 1B

ersetup

Vcc

Vss

Fig. 1C

ersetupb

Vcc

Vss

Fig. 1D

hset

Vcc

Vss

Fig. 1E

hvneg1, hvneg2

Vss

Fig. 1F

hhvpre

Vcc

Vpp

Fig. 1G

hhvpre1

Vcc

Vss

Fig. 1H

hvnpx

Vss

Vpp

Fig. 1I

hnes

Vss

Vnee

Fig. 1J

xwlb

Vss

Vcc

Fig. 1K

xwlb

Vcc

Vss

Fig. 1L

WL0~WL31

Vss

Vpp

Fig. 1M

WL32~

WL16383

Vss

Vnee

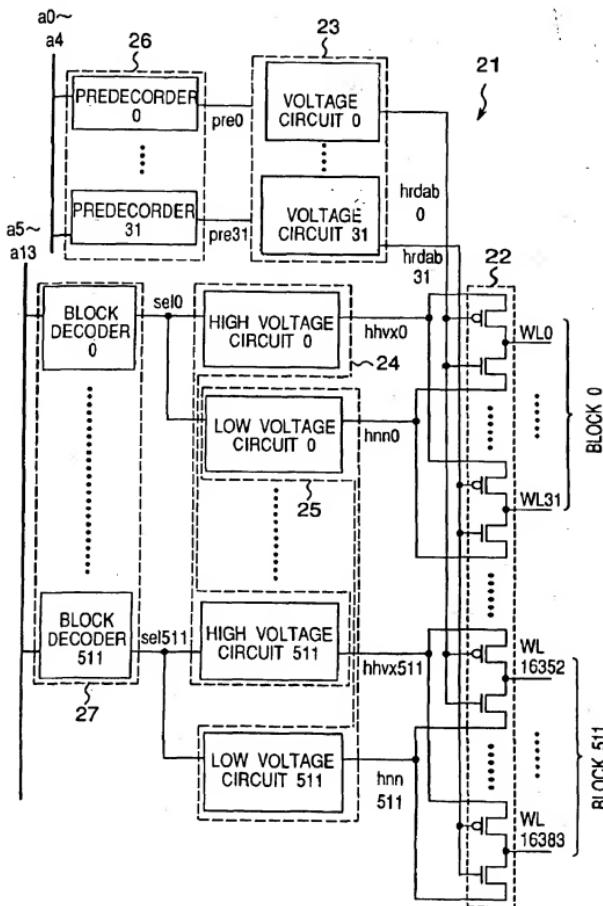
Approved
10/17/03



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SEP 8 2010
U.S. PATENT & TRADEMARK OFFICE

App No.: 09/598,384 Docket N. : 204552018400
Inventor: Yasuaki HIRANO
Title: ERASE METHOD FOR NONVOLATILE
SEMICONDUCTOR STORAGE DEVICE AND ROW
DECODER CIRCUIT FOR FULFILLING THE METHOD

Fig. 12 **REPLACEMENT SHEET**





REPLACEMENT SHEET

Fig. 13

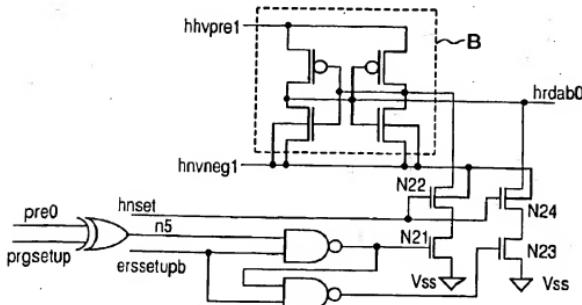
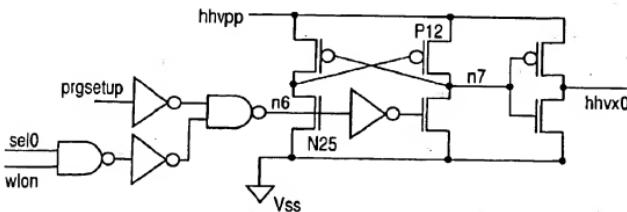


Fig. 14



REPLACEMENT SHEET

Fig.19 PRIOR ART

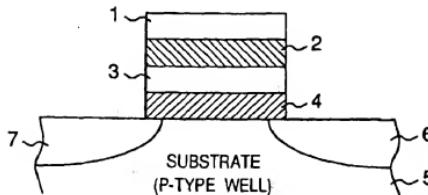
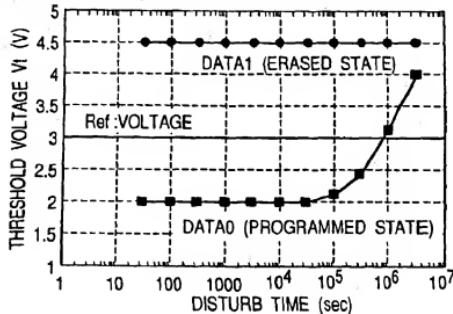


Fig.20 PRIOR ART

CONDITIONS : $V_g=0V$, $V_d=V_s=$ FLOATING , $V_{sub}=-8V$





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Fig.21 PRIOR ART

